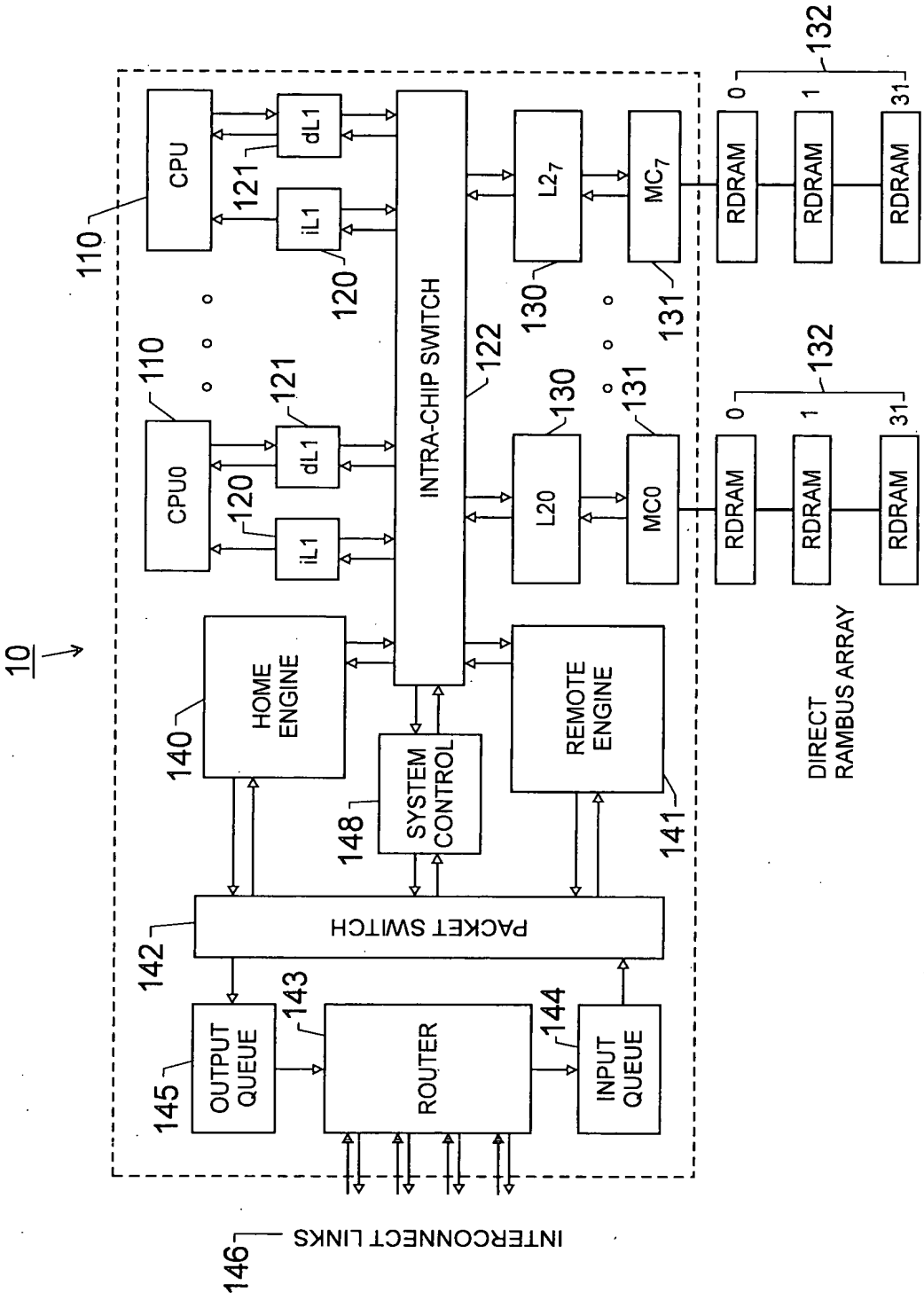
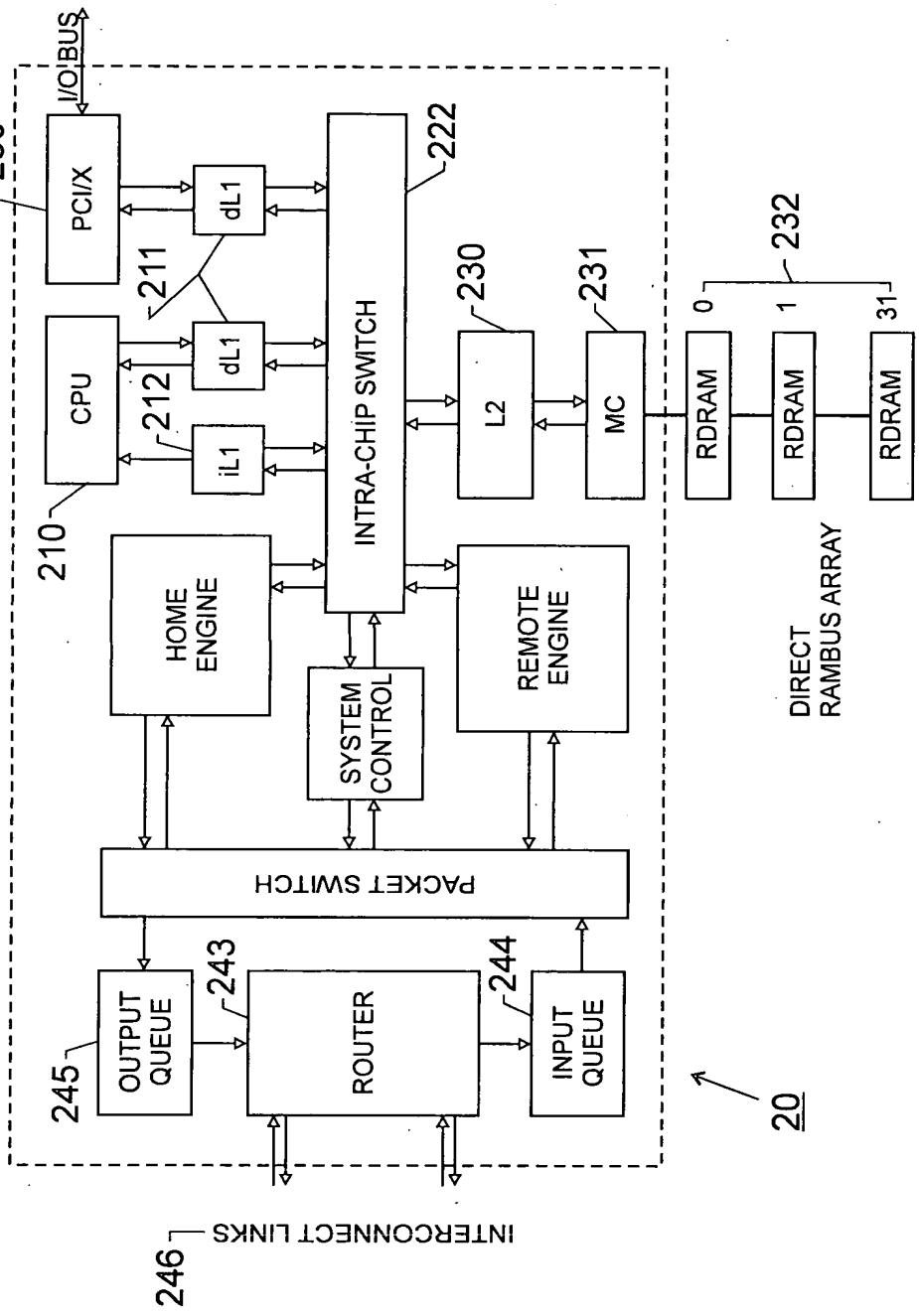


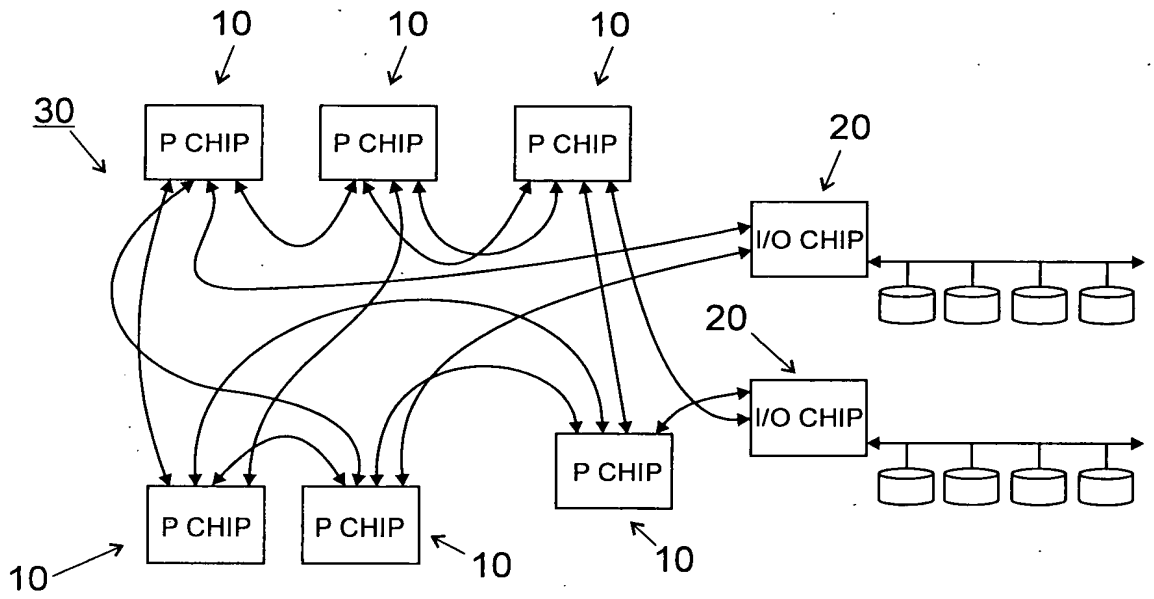
BLOCK DIAGRAM OF A SINGLE-CHIP PIRANHA PROCESSING NODE

FIG. 1



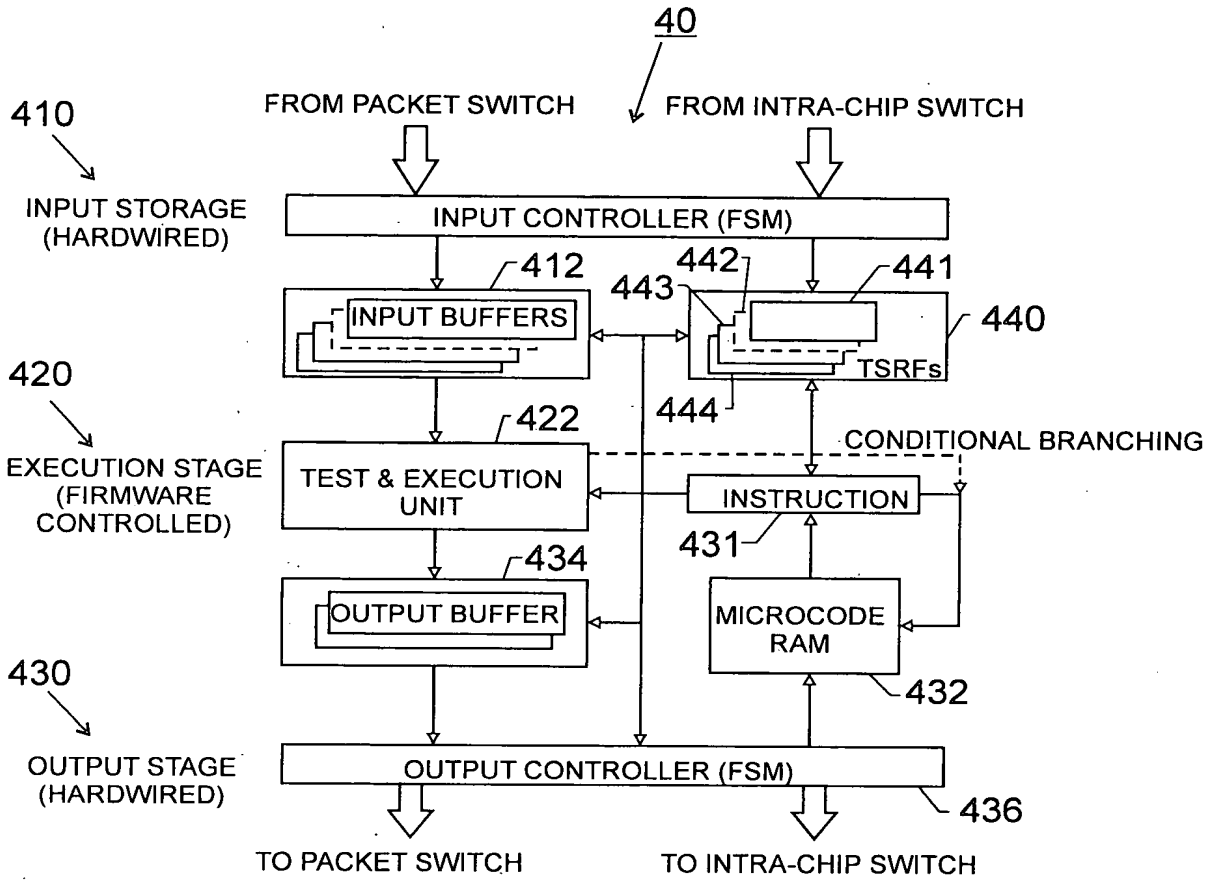
BLOCK DIAGRAM OF A SINGLE-CHIP PIRANHA I/O NODE

FIG. 2



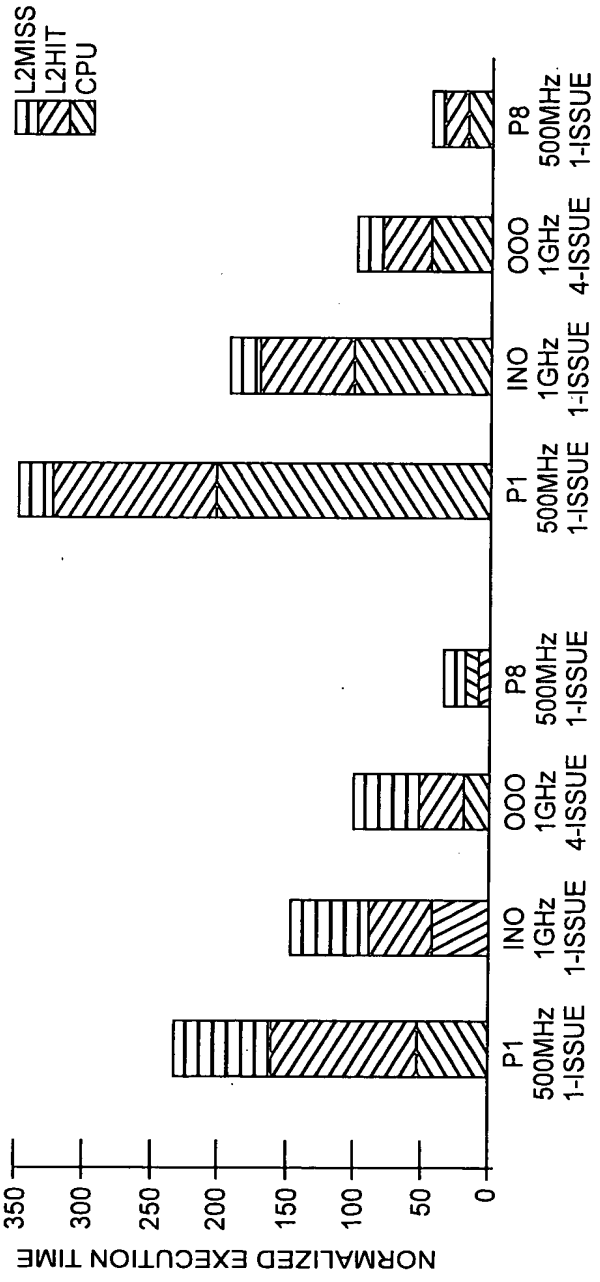
EXAMPLE CONFIGURATION FOR A PIRANHA SYSTEM WITH SIX PROCESSING (8 CPUs EACH) AND TWO I/O CHIPS.

FIG. 3



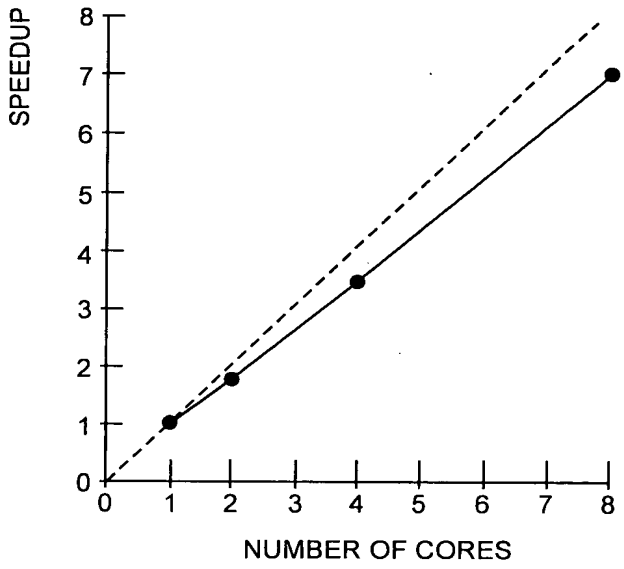
BLOCK DIAGRAM OF A PROTOCOL ENGINE

FIG. 4

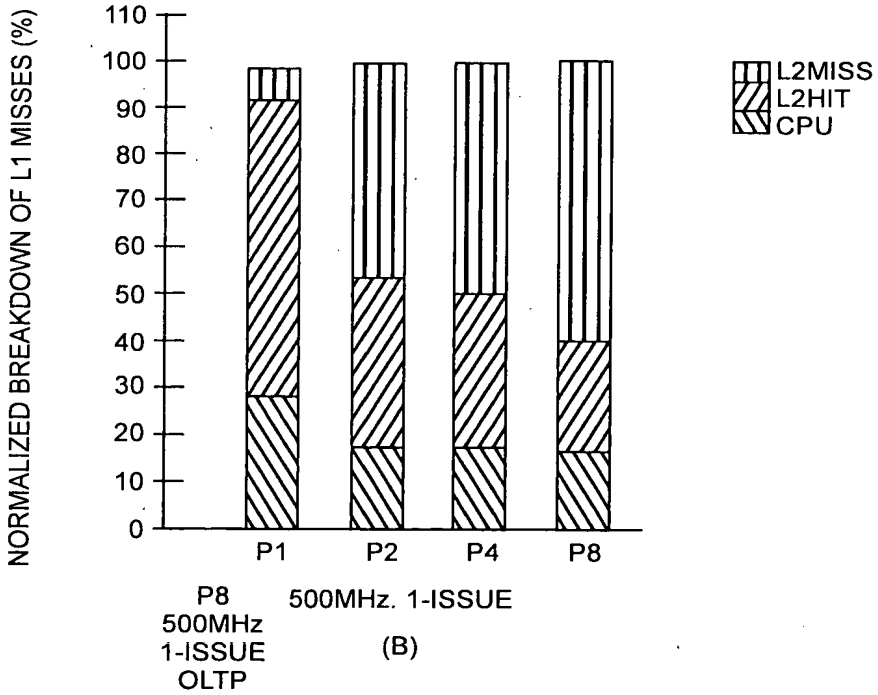


ESTIMATED PERFORMANCE OF A SINGLE-CHIP PIRANHA
(8 CPUs/CHIP) VERSUS A 1GHz OUT-OF-ORDER PROCESSOR

FIG. 5



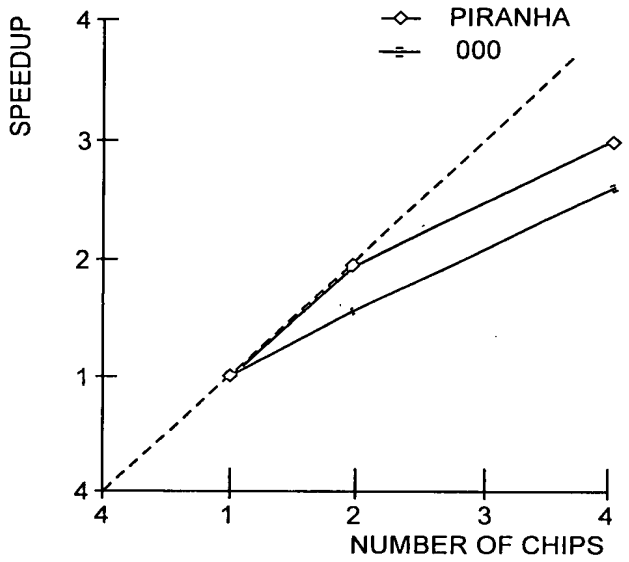
(A)



(B)

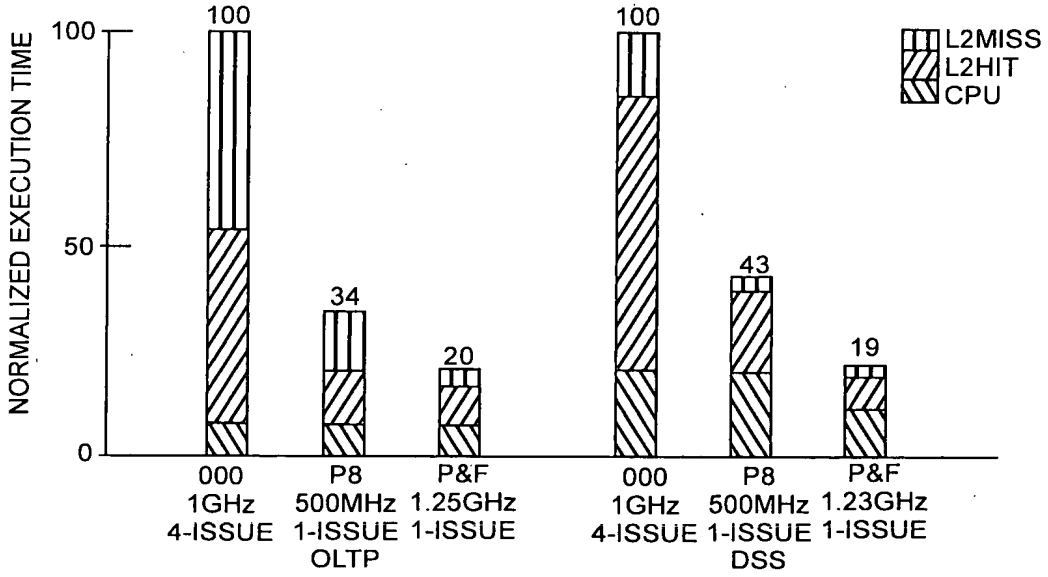
PIRANHA'S (A) SPEEDUP AND (B) L1 MISS BREAKDOWN FOR OLTP

FIG. 6



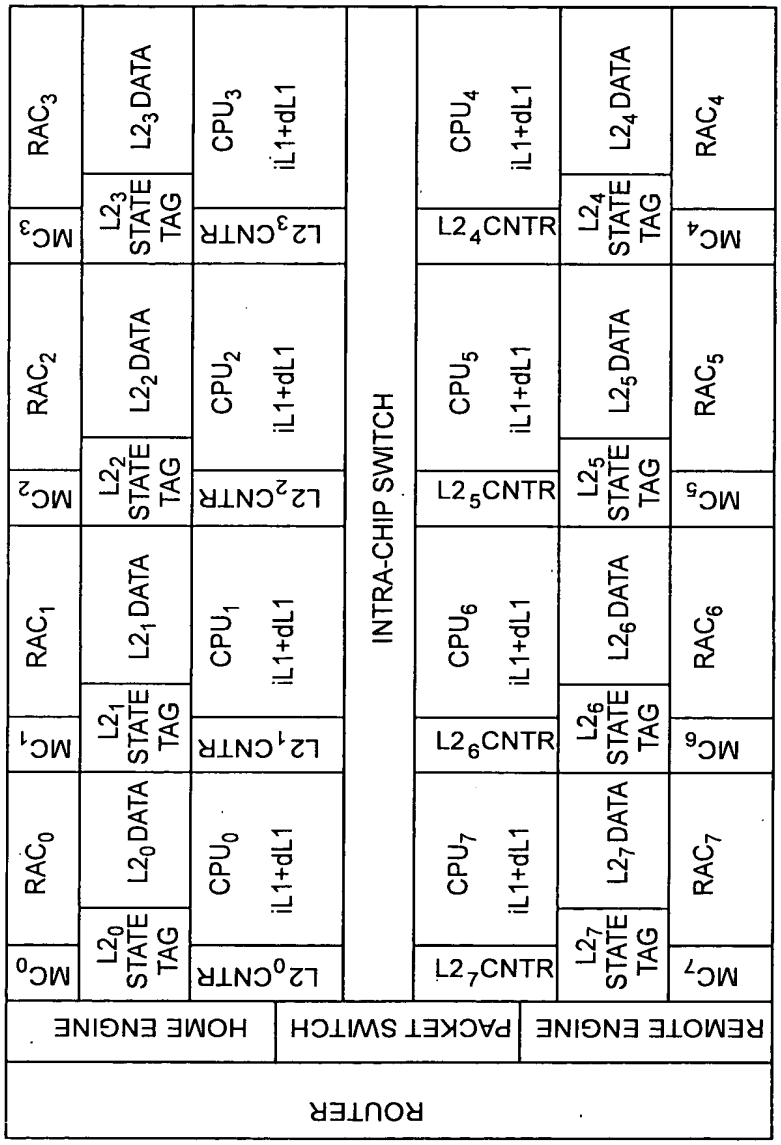
SPEEDUP OF OLTP IN MULTI-CHIP SYSTEMS WITH 500 Mhz 4-CPU PIRANHA CHIPS VERSUS 1 Ghz OUT-OF-ORDER CHIPS. (A SINGLE-CHIP 4-CPU PIRANHA IS APPROXIMATELY 1.5x FASTER THAN THE SINGLE-CHIP 000)

FIG. 7



PERFORMANCE POTENTIAL OF A FULL-CUSTOM PIRANHA CHIP FOR OLTP AND DSS

FIG. 8



FLOOR-PLAN OF THE PIRANHA
PROCESSING NODE WITH EIGHT CPU CORES

FIG. 9